REMARKS

In the Office Action mailed January 14, 2005, claims 16 and 26 are rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. It is suggested that the recitation "wherein the sum of the delays is less than the period of the input clock signal" is not described in the specification. In response to the rejection, Applicant respectfully requests reconsideration. Direct support for the language can be found in paragraph [0006], which in describing how the delay introduced by each of the programmable delay lines is selected with respect to the period of the input clock signal, specifically indicates that "the sum of the delays introduced by the programmable delay lines is less than the period of the input clock signal." Accordingly, Applicant respectfully requests reconsideration of the rejection.

Claims 1-8, 11, 12, 14-17, 21 and 26 are rejected under 35 USC §102(e) as being anticipated by Lacey (U.S. Patent 6,651,181). Claims 18-20 and 23-25 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response to the rejection of the claims in view of Lacey, Applicant respectfully submits that each independent claim distinguishes over Lacey, and respectfully requests reconsideration of the claims. Lacey is directed to a clocking scheme for a programmable logic device. A PLL/CLK multiplexer circuit 100 generates a plurality of global clock signals which "may be presented . . . to every logic element 108a-108n and I/O block 110a-110n in the PLD 102." (Col. 3, lines 7-9). As shown in Fig. 2, a PLL 144 generates phase shifted output clock signals based upon an input clock signal. A circuit 130 (having dividers 150 and multiplexers 152) receives the various outputs of the PLL, and will generate a divided signal based upon the input clock signal, or will select one of the phases of the output clock signal. Circuit 130 will select outputs of the PLL and generate four parallel output signals. Finally, a circuit 132 having four multiplexers 154 will generate four clock outputs by selecting one of (i) an output of circuit 130, (ii) an input clock signal, (iii) a JTAG test clock (TCK) signal, or (iv) JTAGINTEST signal. Finally, Fig. 3 shows clock-to-out time improvements for various phases of the clock when using phase shifted signals generated by a PLL,

compared to when not using a PLL. However, as will be described in more detail below, there is no teaching or suggestion that certain I/O blocks are configured to operate in response to specific clock signals. Rather, each of the independent claims, which will be addressed separately, includes limitations which are clearly not disclosed or suggested by Lacey.

Independent Claim 1

Independent claim 1 is directed to a semiconductor device having a digital clock manager comprising "a plurality of series connected delay elements" coupled to a multiplexer for generating a plurality of clock signals. It is suggested in the Office Action that PLL 144 comprises a plurality of series connected delay elements. However, Applicant respectfully submits that there is no teaching or suggestion that PLL 144 comprises series connected delay elements as claimed.

Claim 1 also comprises input/output blocks which are configured to "operate in response to" specific clock signals. In particular, claim 1 comprises

> "a first set of IOBs configured to operate in response to a first clock signal of the plurality of clock signals, a second set of IOBs configured to operate in response to a second clock signal of the plurality of clock signals, and a third set of IOBs configured to operate in response to a third clock signal of the plurality of clock signals."

It is suggested in the Office Action that the plurality of input/output blocks of Lacey is configured to operate in response to a specific clock signal (e.g. input/output blocks 110a, 110h are configured to operate with a first clock signal GCLK0). However, Applicant does not see any reference in Lacey that specific sets of input/output blocks are configured to operate with specific clock signals. As can be seen in Fig. 1, the logic elements receive the global clock signals by way of the input/output blocks and the horizontal/vertical routing channels 104/106. Lacey merely teaches that a plurality of global clock signals is provided to every logic element 108a-108n and I/O block 110a-110n in the PLD 102. Applicant respectfully submits that there is no teaching or suggestion in Lacey that certain I/O blocks are configured to operate in response to a specific clock signal. Accordingly, Applicant submits that claim 1, and dependent

claims 2-7, distinguish over Lacey.

Independent Claim 8

Independent claim 8 is directed to a method of operating a semiconductor device. Claim 8 includes steps of:

> "operating a first set of input/output blocks in response to a first clock signal of the plurality of clock signals, wherein the first clock signal lags the input clock signal by a predetermined first phase angle; and
>
> operating a second set of input/output blocks in response to a second clock signal of the plurality of clock signals, wherein the second clock signal lags the input clock signal by a predetermined second phase angle."

Lacey fails to disclose or suggest operating different sets of input/output blocks in response to different clock signals, for the reasons set forth above. That is, there is no teaching or suggestion in Lacey that different sets of input/output blocks operate in response to different clock signals.

Independent Claim 16

Independent claim 16 is also directed to a method of operating a semiconductor device, and includes steps of:

> "determining a period of an input clock signal;
> introducing a plurality of discrete delays to the input clock signal, thereby generating a corresponding plurality of delayed clock signals, wherein the sum of the delays is less than the period of the input clock signal; and
> using the plurality of delayed clock signals to control output switching of the semiconductor device."

Applicant respectfully submits that none of the steps of claim 16 is disclosed by Lacey. It is suggested in the Office Action that the determination of a "half cycle" of the input clock signal comprises determining the period of the input clock. Lacey teaches in col. 5, lines 5-12 that a T-type flip-flop could be used to produce an output clock waveform on the I/O pad 162 that is substantially half the frequency of the selected clock signal. However, Applicant respectfully submits that Lacey fails to disclose or suggest determining the period as claimed by Applicant.

Applicant further submits that Lacey fails to disclose or suggest introducing a plurality of discrete delays to the input clock signal as claimed by Applicant. It is suggested in the Office Action that PLL 144 inherently comprises delays such as inverters. However, Applicant claims a step of introducing a plurality of discrete delays such that "the sum of the delays is less than the period of the input clock signal." Applicant further claims using the plurality of delayed clock signals to control the output switching of the semiconductor device. It is suggested in the Office Action that such a switching is an "intended use." However, there is no teaching or suggestion that a "plurality of delayed clock signals" is used "to control output switching of the semiconductor device." Accordingly, Applicant respectfully requests reconsideration of the rejection of claim 16. Applicant further submits that dependent claims 17-20 are not disclosed by Lacey, and are also allowable over Lacey for the same reasons that independent claim 16 is believed allowable.

Independent Claim 21

Independent claim 21 is directed to a semiconductor device having a plurality of series-connected programmable delay lines and delay control circuitry. In particular, the delay control circuitry is configured to "program a delay in each of the plurality of series-connected programmable delay lines in response to the period of the input clock signal." It is suggested in the Office Action that the PLL 144 of Lacey inherently discloses the plurality of series connected programmable delay lines, and that the circuit 130 of Lacey discloses a delay control circuitry. However, Applicant respectfully submits that a plurality of series-connected programmable delay lines is not inherent to a PLL. More importantly, circuit 130 does not program a delay in each of the plurality of series-connected programmable delay lines as claimed by Applicant. Rather, circuit 130 of Lacey receives a plurality of outputs of the PLL, and alters the outputs of the PLL (i.e. divides the output clock of the PLL and/or selects a phase of the output of the PLL). That is, circuit 130 generates parallel outputs of phase signals generated by a PLL, but clearly does not program a plurality of series-connected programmable delay lines. Accordingly, Applicant respectfully requests reconsideration of independent claim 21, and submits that dependent claims 22-25 are allowable for the same reason

that independent claim 21 is believed allowable.

Independent Claim 26

Finally, independent claim 26 is directed to a semiconductor device comprising:

> means for determining a period of an input clock signal;
> means for introducing a plurality of delays to the input clock signal, thereby generating a corresponding plurality of delayed clock signals, wherein the sum of the delays is less than the period of the input clock signal; and
> means for using the plurality of delayed clock signals to control output switching of the semiconductor device.

Applicant respectfully submits that Lacey fails to disclose the means elements of claim 26 for the same reasons set forth above with respect to the steps of the method of claim 16.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 12, 2005.

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